

Laboratory #12

Digital Circuits

I. Objectives

1. Learn the concept of D-flip flop, counter, ramp generator
2. Learn how to use the digital channel of oscilloscope to measure

II. Components and Instruments

1. Components
 - (1) Counter IC: 74LS163 ×1
 - (2) NAND IC: 74HC08 ×2
 - (3) CD4007 ×1
 - (4) Resistor: 10kΩ ×5, 20kΩ ×4, 1MΩ ×1
 - (5) Capacitor: 330pF ×2
 - (6) Crystal: DT26 ×1
2. Instruments
 - (1) DC power supply (Keysight E36311A)
 - (2) Oscilloscope (Agilent MSOX 2014A)

III. Reading

1. Section 15.1, 17.1, of “Microelectronics Circuits 7th edition, Sedra/Smith”.

IV. Preparation

1. Fundamentals of CMOS logic gate

By the mid-1950s, the first logic gate, comprised of bipolar junction transistors (BJTs), were commercially available. It was a very important key to lead to the first digital integrated circuits (ICs) in the early 1960s. Until the early 1980s, the digital IC using BJTs was the dominant design. However, Because of power dissipation and the requirement based on Moore’s law to pack more and more transistors on a single IC chip, BJT is replaced by NMOS, and NMOS by CMOS, again predominantly. Today, CMOS represents 98% of newly designed digital systems. In other words, CMOS logic circuit is the fundamental component in a variety of digital ICs.

In electronic, A CMOS logic gate, implementing a Boolean function, is the fundamental component of digital integrated circuits. Its logic operation is to turn one or more binary inputs into a single binary output.

In this section, fundamental static CMOS logic gates namely NOT, NAND,

NOR, are introduced and explain their operation based on Boolean function. The purpose is to understand how logic gate can be implemented by using arrangement of CMOS.

(1) CMOS inverter

The block representation of the CMOS inverter is shown in Fig. 12.1 (a). And, Fig. 12.1 (b) is shown that the CMOS inverter is comprised of one NMOS transistor and one PMOS transistor.



Fig. 12.1 (a) Block representation of the inverter

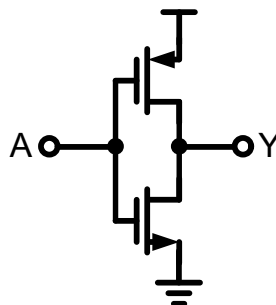


Fig. 12.1 (b) Schematic of the CMOS inverter

The logic function of the CMOS inverter is expressed by Boolean equation which be as follow:

$$Y = \bar{A} \dots\dots(\text{Eq. 12.1})$$

When the input A is 0, the NMOS transistor turns off and the PMOS transistor turns on. Therefore, it leads the output Y to be pulled up to 1 due to the connection between Y and V_{DD} . In contrast, When the input A is 1, the NMOS transistor turns on and the PMOS transistor turns 0, and the output Y will be pulled down to 0 due to the connection between Y and GND. In other words, the CMOS inverter inverts the logic value of its input code. Table 12.1 summarizes the operation result of NOT gate.

Table 12.1 Truth table of the inverter

A	Y
0	1
1	0

Based on the analysis of CMOS inverter, the generalization is that the inverter is comprised of a NMOS pull-down transistor and a PMOS pull-up transistor. Therefore, CMOS logic-gate circuit includes two networks which are NMOS pull-down network and PMOS pull-up network, respectively. Representation of general logic gate using pull-down and pull-up networks is shown in Fig.-12.1 (c).

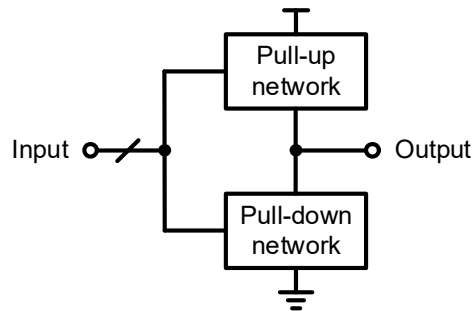


Fig. 12.1 (c) General logic gate using pull-down and pull-up networks

The pull-down network lead output node to be pulled down to GND causing the logic-0 to appear at the output. On the other hand, the pull-up network lead output node to be pulled up to V_{DD} causing the logic-1 to appear at the output. The concept can also be used in NAND gate and NOR gate.

(2) 2-input NAND gate

The block representation of 2-input NAND gate is shown in Fig. 12.2 (a). And, Fig. 12.2 (b) is shown that 2-input NAND gate is comprised of two series NMOS transistors between Y and GND and two parallel PMOS transistors between Y and V_{DD} .



Fig. 12.2 (a) Block representation of the 2-input NAND gate

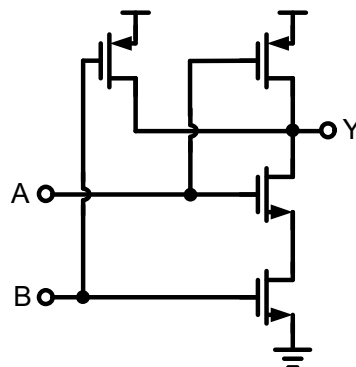


Fig. 12.2 (b) Schematic of the 2-input NAND gate

The logic function of the NAND gate is expressed by Boolean equation which be as follow:

$$Y = \overline{A \cdot B}$$

If either input A and B is 0, at least one of NMOS turn off, so output Y is pulled up to 1 due to the disconnection between Y and GND. If both input A and B are 1, all PMOSs turn off. Therefore, Y is pulled down to 0 due to the disconnection between Y and V_{DD} . The truth table of the NAND gate is given in Table 12.2.

Table 12.2 Truth table of the NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(3) 2-input NOR gate

The block representation of 2-input NOR gate is shown in Fig. 12.3 (a). And, Fig. 12.3 (b) is shown that 2-input NOR gate is comprised of two parallel NMOS transistors between Y and GND and two series PMOS transistors between Y and V_{DD} .

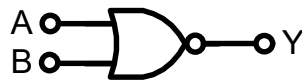


Fig. 12.3 (a) Block representation of the 2-input NOR gate

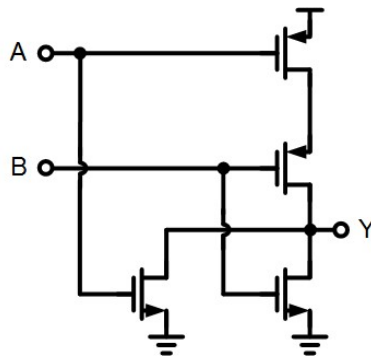


Fig. 12.3 (b) Schematic of the 2-input NOR gate

The logic function of the NOR gate is expressed by Boolean equation which be as follow:

$$Y = \overline{A + B}$$

If either input A and B is 1, at least one of PMOS turn off, so output Y is pulled down to 0 due to the disconnection between Y and V_{DD} . If both input A and B are 0, all NMOSs turn off. Therefore, Y is pulled up to 1 due to the disconnection between Y and GND. The truth table of the NOR gate is given in Table 12.3.

Table 12.3 Truth table of the NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

2. Latches and D-FlipFlops

Application of CMOS logic-gate circuit can be categorized into combinational circuits and sequential circuits. In digital-circuit theory, combinational circuits, such as full adder, multiplexer, encoder, decoder, and so on. Their outputs depend on present input rather than the history of the input. In other words, this type circuit has not memory. Therefore, the advanced application are sequential circuits. Their output depend not only the present input but also the previous input. Thus sequential circuits has the property of information storage.

One approach of sequential circuit for providing memory (information storage) to a digital ICs is the bistable circuit. A bistable circuit based on the application of positive feedback is used to store one bit of information. It has two stable states: one stable state is to store 0, and the other is to store 1. Bistable circuits are the category of static sequential circuits because they always remain either stable state. In next section, the concept of basic bistable circuit, latch, and its application, flip-flop, will be introduced and explained.

(1) The Latch

The inverter-based latch shown in Fig. 12.4 (a), is the basic memory component. It is comprised with two cross-coupled inverters and based on positive-feedback loop.

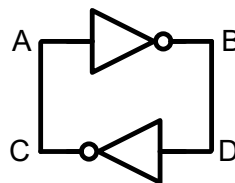


Fig. 12.4 (a) Schematic of the basic latch

In order to observe the operation of inverter-based latch, the feedback loop connected between input and output of one inverter is broken, as shown Fig. 12.4 (b). Based on Fig. 12.4 (b), we can determine the voltage-transfer characteristic (VTC), as shown in Fig. 12.4 (c), of inverter-based latch. VTC indicates three operating point, namely two different stable operating mode and one unstable operating mode.

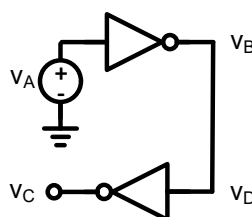


Fig. 12.4 (b) The basic latch with feedback loop opened

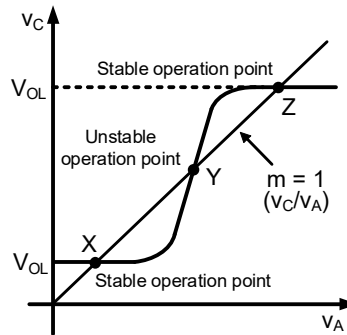


Fig. 12.4 (c) Operating points of the latch

In Fig. 12.4 (c), it indicates that the straight line with unity slope intersects at X, Y and Z which can serve as operating points of the latch. Among all these operating points, point Y is unstable operating point, the latch cannot work at any long period time. Unstable point Y may occur by electrical interference /noise which presents inevitably in any circuit due to positive feedback. Points X and Z are stable operating points which the latch circuit always remain either stable state. One of the stable states corresponding to operating point X indicates that the output v_B is high (at V_{OH}) and the output v_C is low (at V_{OL}) when input v_A is low. The other of the stable states corresponding to operating point Z indicates that the output v_C is high (at V_{OH}) and the output v_B is low (at V_{OL}) when input v_A is high. Therefore, the latch has the bistable property with two complementary outputs. And, the latch changes to another state by the specific trigger signal.

(2) D-flip flop circuits

In electronics, a flip flop is an application circuit of the latch and can be used to do the state information storage. The flip flop is a bistable multivibrator which can change the state of the circuit by inputting one or more control signals. There are a variety of types of flip flops, including data-type flip-flop (D-flip flop), toggle flip flop (T flip-flop), JK-flip flop, etc. Among these types, D-flip flop is the most popularly used in the digital ICs due to the application of data storage/transfer and delay line. The block diagram of D-flip flop is shown in Fig. 12.5. It is comprised with two inputs including the data input data D and the clock ϕ and two outputs including Q and \bar{Q} .

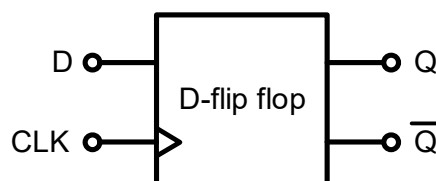


Fig. 12.5 Block diagram of D-flip flop

Furthermore, the simple circuits are the important target of digital ICs. Therefore, the circuit implementation of D-flip flop is shown in Fig. 12.6 (a).

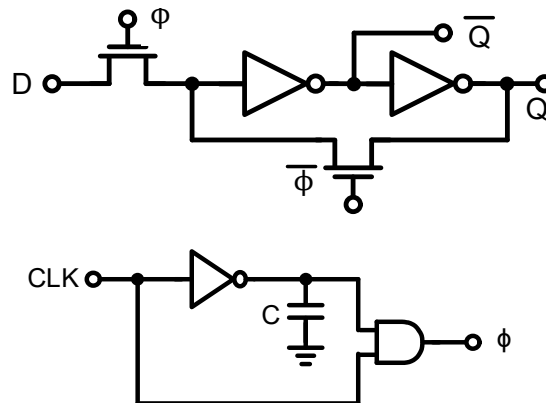


Fig. 12.6 (a) Schematic of D-flip flop

This simple implementation is comprised of two switches and two CMOS inverter connected in a positive feedback loop, namely basic latch in Fig. 12.4 (a). The operation of this circuit: When the clock (CLK) changes from 0 (low) to 1 (high), the rising edge detector generates the output (ϕ) a pulse wave. It will cause the input D to be connected to the input of the first inverter and the loop is opened. The capacitance at the input of the first inverter is charged by D value, and the capacitance at the input of the second inverter is charged by \bar{D} value. Therefore, the outputs Q and \bar{Q} depends on the value of D. Conversely, when CLK event is not rising edge, the path between the input D and D-flip flop is broken. Meanwhile, the loop is closed, and the latch gets the state based on the value of D before ϕ is 0.

From above analysis, the D-flip flop in Fig. 12.6 (a) combines the positive feedback loop of basic latch circuit and charge-storage technique of dynamic circuits. It is critical to care that the ϕ and $\bar{\phi}$ cannot simultaneously high at any time. In other words, these two clocks phase is non-overlapping, as shown in Fig. 12.6 (b).

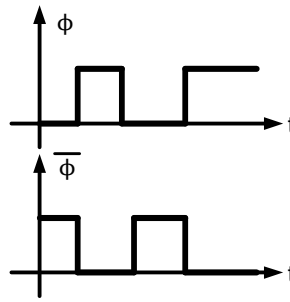


Fig. 12.6 (b) Waveform of non-overlapping clock

3. 4-bit counter

With the aforementioned basic circuits, a large amount of more complex building blocks of digital calculation, including adder, multiplexer, multiplier, etc. can be achieved by the combination of basic circuits. Binary counter is one of these applications. The function of a synchronous counter is generating a counting-up or down sequential code at its output. Each clock pulse applied to the clock input increments or decrements the number in counter. The general purpose of synchronous counter is storing the number of times a particular event has occurred or ended in relationship to a clock signal. Fig. 12.7 shows the block diagram of a 4-bit synchronous counter. It consists of four JK flip-flops, two AND gates and one clock generator.

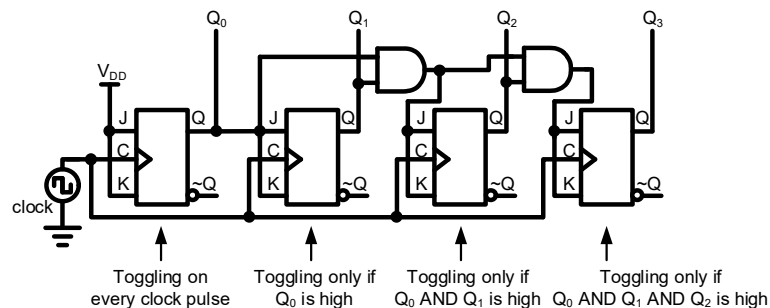


Fig. 12.7 4-bit synchronous up counter

According to Fig. 12.7, the external and same clocks are fed directly into each JK flip-flop. Therefore, the state of all flip-flops changes at the same time. In the first JK flip-flop, the input J and K are connected to V_{dd} . An idea of this synchronous counter is to let the each flip-flop invert when all less significant bits are logic-high state. For example, Q_1 is inverted when Q_0 is high; Q_2 is inverted when Q_0 and Q_1 is high, and so on. Based on this idea, we can realize the logic function of the counter circuit using the flip flop.

Furthermore, a JK flip-flop of 4-bit synchronous up counter, as shown in Fig. 12.7, can be constructed by a D flip-flop, one OR gate, two AND gates and one inverter. The schematic and truth table of JK flip-flop which is derived from D

flip-flop can be shown in Fig. 12.8, Table 12.4, respectively.

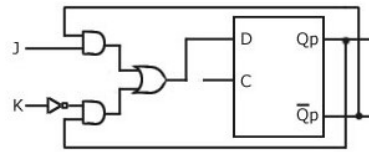


Fig. 12.8 D flip-flop-based JK flip-flop

JK input		Output		D input	Comment
J	K	Q_p	Q_{p+1}	D	
0	0	Q	Q	Q	Hold
0	1	Q	0	0	Reset
1	0	Q	1	1	Set
1	1	Q	\bar{Q}	\bar{Q}	Toggle

Table 12.4 Truth table of D flip-flop-based JK flip-flop

4. Ramp generator (the application of 4-bit counter)

One characteristic of this kind of counter is that once the output overflows (counting-up) or underflow (counting down), the output will be reset. Due to the characteristic, a ramp generator can be implemented by a counter with a R-2R ladder as a simple digital-to-analog converter. By R-2R theory, the resistance is equivalent to R no matter looking left or right. Thus the incremental at the output is binary weighted. The schematic of ramp generator is shown in Fig. 12.9.

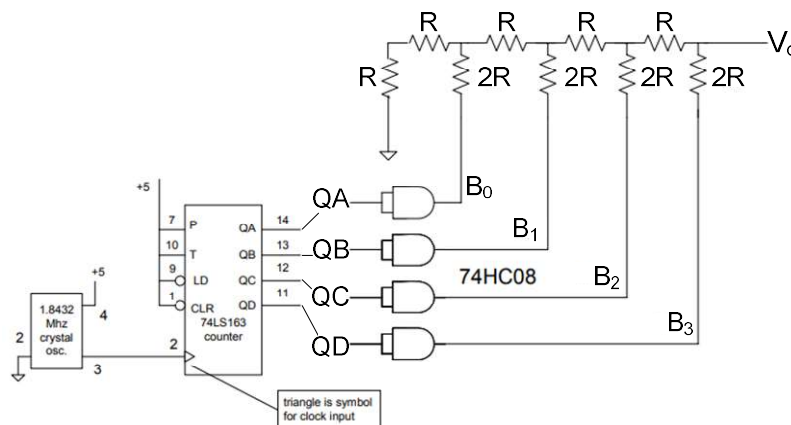


Fig. 12.9 Ramp generator

V. Exploration

The connections of 74LS163 IC are shown below.

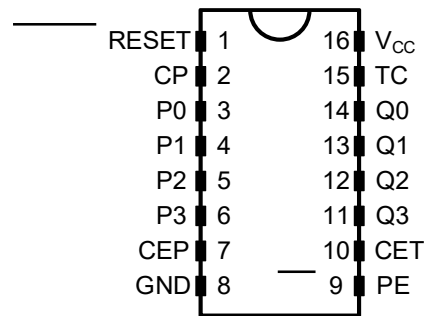


Fig. 12.10 Pin diagram of 74LS163

NOTE: Pin16 must be connected to the most positive voltage, and pin 8 to the 0. For the sake of safety, maintain the voltage between pin 16 and pin 8 at or below 5V to avoid internal voltage breakdown. **Make sure you turn off the power supply before changing any circuit connection.**

The layout and connections of 74HC08 IC are shown below.

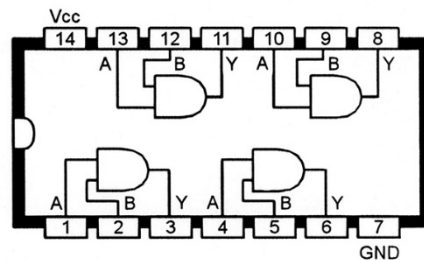


Fig. 12.11 Pin diagram of 74HC08

NOTE: Pin14 must be connected to the most positive voltage, and pin 7 to 0. For the sake of safety, maintain the voltage between pin 14 and pin 7 at or below 6V to avoid internal voltage breakdown. **Make sure you turn off the power supply before changing any circuit connection.**

1. 4-bit counter

- (1) Assemble the circuit in Fig. 12.12, using the 74LS163. The clock CLK is provided by crystal oscillator of Lab8 in clock generator.
- (2) Use the digital channel of the oscilloscope to measure the output of counter

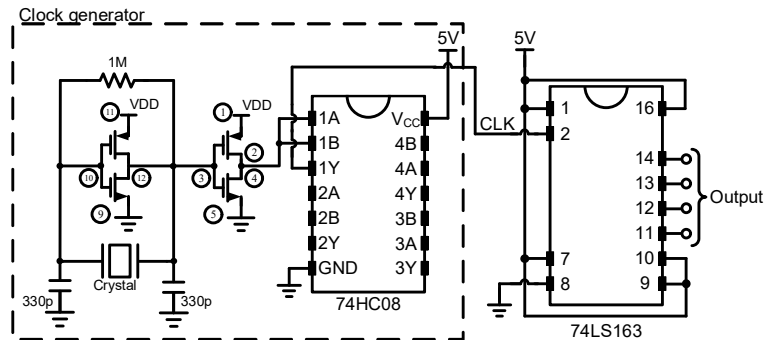


Fig. 12.12 Circuit connection of 4-bit counter

2. Ramp generator

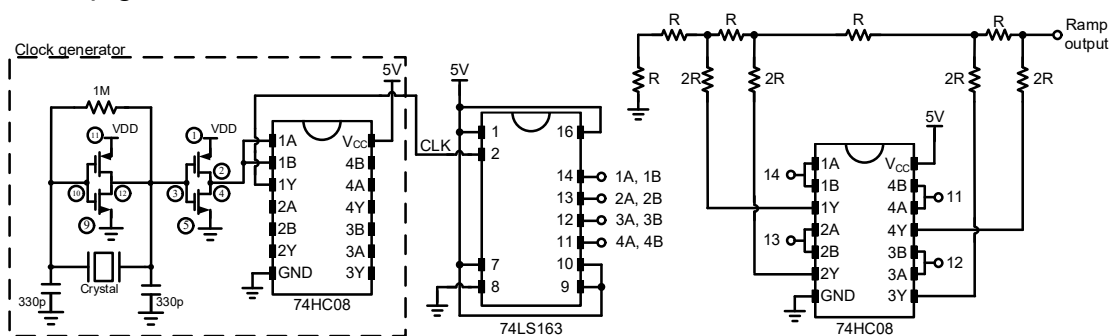


Fig. 12.13 Circuit connection of 4-bit counter based on Fig. 12.9

- (1) Assemble the circuit in Fig. 12.13, using the 74LS163 and 74HC08 ICs. The clock CLK is provided by crystal oscillator of Lab8 in clock generator. The parameters are: $R=10k\Omega$.
- (2) Use the analog channel of the oscilloscope to measure the output of ramp generator.

VI. Reference

1. "Microelectronic circuit", seven edition.
2. "74HC08" datasheet. (<https://www.diodes.com/assets/Datasheets/74HC08.pdf>)
3. "74LS163" datasheet. (<http://users.ece.utexas.edu/~valvano/Datasheets/74LS163.pdf>)

Laboratory #12 Pre-lab

Class:

Name:

Student ID:

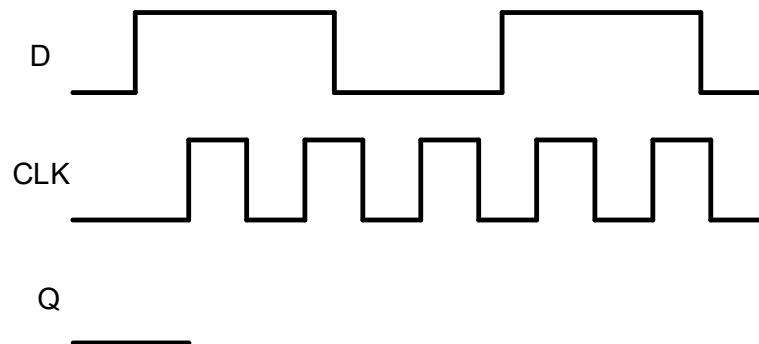
1. Problem 1 (Datasheet reading)

Download the datasheet of 74HC08 IC (the website is listed in Ref [2]), then read and answer the following questions:

- (1) What's the range of supply voltage?
- (2) What's the Boolean function?

2. Problem 2 (Operation Analysis)

According to Fig. 12.6, please briefly explain the operation of D flip flop. And then, please plot the output (Q) waveform of D flip flop based on the below figure.



3. Problem 3 (Datasheet reading)

Download the datasheet of 74LS163 IC (the website is listed in Ref [3]), then read and answer the following questions:

- (1) What's the range of supply voltage?
- (2) What's the function of pin1~pin16?

Laboratory #12 Report

Class:

Name:

Student ID:

1. Exploration 1

(1) Output waveforms:

2. Exploration 2

(1) Output waveforms:

3. Problem 1

Please briefly explain the truth table based on Table 12.4

4. Problem 2

Please briefly explain how to generate ramp waveform using 4-bit counter.

5. Conclusion